ACCEPTED: A. Beg and W. Ibrahim, "Relating Reliability to Circuit Topology," in IEEE North Eastern Workshop on Circuits and Systems (NEWCAS'09), Toulouse, France, 2009

Relating Reliability to Circuit Topology

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Abstract **- Reliability analysis of nano-scale circuits can be done using different techniques, one of them being Bayesian networks. Using this scheme, the relationship of circuit's topology to reliability has been studied for several thousand randomly generated (combinational) 3 to 9 variable circuits; the circuits contained up to 40 gates in up to 10 tiers/levels. As anticipated, strong, positive correlations were found between gate counts and circuit's probability of failure (PF), and between the level counts and circuit PF. However, the input counts and the circuit PFs were weakly correlated. These findings can be useful in creating reliability models for arbitrary circuits.**

I. Introduction

Nanotechnology is expected to be one of the most important technologies of 21st century. New nanomaterials and nanodevices will have a major impact in all areas of the global economy. The nanotechnology is inherently interdisciplinary, combining fields such as physics, chemistry, biology, computer science, and manufacturing. Some of the industries impacted by nanotechnology include pharmaceuticals, medical, biotechnology, aerospace and aviation, defense, automotive, computers, semiconductors, information technology, communications, and energy. Due to its wide scope, nanotechnology has the potential to create an industrial revolution that will have a major impact on society and our everyday life, comparable to information technology of the 20th century.

In the semiconductor sector, the nano-era started in 2002 with the introduction of the 90nm process by IBM. This was followed in 2006 by 65nm process in a variety of Intel microprocessors. In 2007, Intel started the mass production of 45 nm chips. Scaling the semiconductor technology deep into the nano-scale will lead to new classes of applications that include wireless sensor networks, wearable computers, implantable devices, etc. The application space is quickly becoming much larger, encompassing: ticketing, check-out counters, warehouse inventory tracking/management, shipping verification, location sensing, patient monitoring, machine-mounted sensing, building climate control, and security. The implantable systems in particular hold great promise for health applications: pace makers, defibrillators and hearing aids being already in use, while retina, ear, and neural implants are starting to be offered. The emergence of these real life applications depends to a great extent on the ability to fabricate/manufacture *small, ultra low power, highly reliable electronic circuits*.

The development of ever-smaller devices brings promise for further improvement in the performance of future integrated circuits (ICs) (reduced size and power consumption), yet also leads to several new technical challenges, including *the need for architectures that reduce the uncertainty inherent to computations at very small scales* [1]-[4]. In particular, as feature sizes are aggressively scaled, the processing of ICs becomes more complex and inevitably introduces more defects. The devices' small sizes, and consequently the tiny amounts of energy required and allowing their switching, make them susceptible to transient failures [5], [6]. Architectures built from emerging nanodevices, such as scaled CMOS, SET (Single Electron Technology/Transistor), Carbon nano-tubes, Silicon nano-wires, molecular devices, spin transistor, etc., will be even more susceptible to parameter variations, fabrication defects, and transient failures induced by environmental/external cause [1],[4].

Therefore, there is currently a clear message coming form the semiconductor industry that *design-for-reliability needs help* [7]. An accurate calculation (estimation) of the reliability of nano-circuits through simulations is essential for future designs. It would help in designing/selecting the most suitable (nano) architecture that optimally trades delay, power, and area versus reliability requirements. Hence, there will be a growing need to accurately estimate reliability/yield [8].

Nano-reliability is defined as the probability that a nano-metric circuit performs its desired functionality without failing for a given amount of time under specified conditions. When the physical sizes of devices are reduced to nano-scale, dramatic changes in device properties start to appear. Reliability of such devices is being studied extensively these days. Failures in nano-scaled circuits can be traced back to a combination of electrical, thermal, chemical and mechanical origins [9]-[10].

The purpose of this paper is to investigate how the reliabilities of nano-metric circuits are affected by the circuit topology. We first briefly describe the related work. Then we present our experimental methodology. After that the data acquired by using a recent reliability calculation tool are presented. And finally we discuss the findings and our future work.

II. Related Research

Choi and Iyer [11] introduced an integrated approach involving switch-level and device-level Monte Carlo simulations to accurately predict the reliability of the circuits. Their method first collects trace data from switch-level simulator; the traces are then utilized in Monte Carlo simulations in order to model dynamic wear-out due to electro-migration and gate-oxide breakdown.

Unlike older fault simulators that mostly targeted single stuck line physical faults, Al-Assad and Hayes [12] presented a hybrid design-error-and-fault-simulator. They combined the two techniques: single-fault propagation and parallel-pattern evaluation. The tool first generates tests (by greedy algorithm), and then performs output dependency evaluation between two outputs. The tool's netlist translator output can be directly used for synthesis purposes.

Miskov-Zivanov and Marculescu [13] proposed using binary decision diagrams and algebraic decision diagrams for analyzing circuit reliability. Their methodology unified analysis of latching-window with electrical and logical masking and treated them as joint dependencies (unlike their independent treatment in the past) on input vectors and circuit configurations. Their scheme lacked the ability to include all values of propagation delays in different paths.

A probabilistic single-event upset (SEU) fault model presented by Rejimon and Bhanja [14] employed logic induced fault encoded directed acyclic graph structured probabilistic Bayesian networks. The model accounts for all spatial dependencies caused by a circuit. The authors reported 5 times faster estimation of SEU faults using this approach, for ISCAS-85 benchmark circuits.

Tosun et al. [15] approach integrated reliability along with the traditional area and timing metrics. Their hardware-software co-design methodology searches through a library of design alternatives in order to yield a design with the best reliability figures. Their proposed framework first finds the most reliable configuration and then tries to meet the area and timing constraints. Although, not mentioned in [15] explicitly, this approach can also be applied to sub-10 nm designs.

In [16], an analytical model for estimating a circuit's sensitivity to SEUs was developed. The model was proposed as a fast alternative to time-consuming Spice simulations. The model, a function of gate delay, approximates the behavior of a single-event transient and how it propagates through the circuit.

The phenomenon of smaller transistor geometries and lower supply voltages causing soft errors in CMOS transistor was modeled in [17]. The authors showed it was possible to use birth-death queue model soft error prediction over a wide time scale. They also stated such predictions could not be made with Spice models.

In [18], Beg devised a method for calculating exact reliability using probability transfer matrices (PTMs). His tool (*AutoPTMate*) created Matlab m-files for given circuits. However, due to their large computational needs (memory) PTMs methodology is only useful for small circuits. To handle larger circuits, Ibrahim et al. [19] introduced a tool called *nano-CR-EDA* that used Bayesian network (BN) numerical method to accurately calculate circuit reliability and to accurately estimate the PF of circuit outputs.

III. Experimental Setup and Data Collection

We used a Perl script to randomly generate more than 8000 Verilog files which described 3 to 9-input (variable) combinational circuits as minterms. The circuits were synthesized (and optimized for area) using Synopsys Design Compiler (SDC) [20], which uses static timing analysis to calculate the timing of the paths in the design. SDC splits the design into number of paths and then optimizes them according to the given design constraints. We used a public domain library (0.35um rev1.3.1) provided by CMU with the following parameters: Operating condition = nom_pvt; process = 1.00; temperature = 90°F; voltage = 3.3V; and interconnect model = balanced_tree.

The synthesized/optimized circuits had 2 to 40 gates in 2 to 10 tiers/levels. The circuits comprised a mix of NOT, OR, NOR, AND, and NAND gates. We had to discard many optimized circuits, for example, the ones that consisted of less than two gates. So we were left with 5184 circuits. Using *nano-CR-EDA* [19], the PF data was collected for all 5184 circuits. Device PF values of 10^{-4} and 10^{-2} were used for calculations. A total of 15,552 tool-runs were made. The data collection required more than 3 months on a Windows-Vista-based x86 machine (Intel Core-2 CPU-6400, 2.13 GHz, 4 GB RAM).

IV. Results and Analysis

The data acquired from reliability tool runs provided some useful insight into how the topologies of circuits affect their reliability. In the first experiment we studied the sensitivity of the circuit reliability to the circuit size (number of gates). In Figs. 1 and 2 the circuit PF is plotted (as circles) against the gate count. Device PFs of 10^{-4} and 10^{-2} are used in the figures. It is clear that as the number of gates increases, the PF of circuits go higher. In numeric terms, positive correlations were found as given in Table I. Device PF of 10^{-2} exhibits a wider envelope and lower correlation.

In Figs. 1 and 2, the solid lines indicate circuit PF is roughly estimated analytically by the equation [21]:

$$pf_{\text{CIRCUIT}} = 1 - \left(\left(1 - \varepsilon\right)^n \right)^m , \qquad (1)$$

where m is the number of gates, n is the number of devices (transistors) per gate, and ε is the device PF.

For lower values of device PF (i.e. 10^{-4} in Fig. 1) the equation provides worse PF estimates than BN-based method. However, as gate PF goes higher (i.e. 10^{-2} in Fig. 2), the equation-based values turn out to be more conservative than BN tool.

How circuit tiers (levels) affect circuit PFs are shown in Figs. 3 and 4. Overall, the data takes the same shape as the ones in Figs. 1 and 2. Here again, high values of positive correlation are found between tier count and circuit PFs. (See Table I).

The effect of number of inputs (variables) on circuit reliability is shown in Figs. 5 and 6. We observe once again, a

positive correlation between input count and circuit PF, although much lower than the previous two cases (gate count and tier count).

The graphs (in Figs 1-6) point to the need of a multi-variable, non-linear model for estimating (if not accurately calculating) circuit reliability, contrary to gate-count based equation (1). The model should also provide values for upper and lower bounds of reliability to better reflect the envelope-like nature of data.

As one can notice, the two-dimensional graphs in Figs. 1-6 are rather simplistic representations of a seemingly high-dimensional topology-reliability relationship. The authors are looking for the answers to the following questions: Which gate types make up better circuits (in terms of circuit reliability) than others? Are single-gate-type (for example, NAND-only, or NOR-only) circuits more reliable than mixed gates used in the current experiments? Can a machine model be built for estimating the circuit reliability (in terms of circuit topology)?

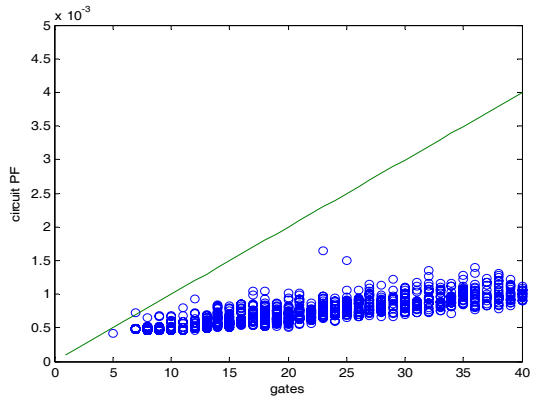

Fig. 1. Effect of gate count on circuit PF when device PF is 10^{-4}

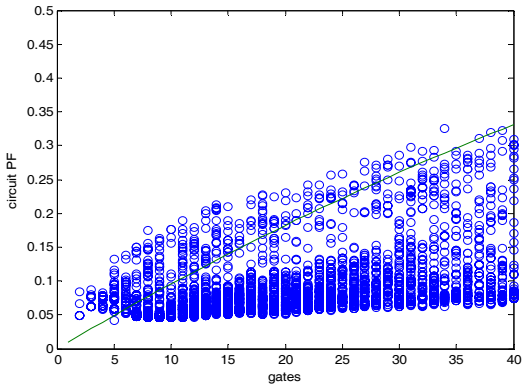

Fig. 2. Effect of gate count on circuit PF when device PF is 10^{-2}

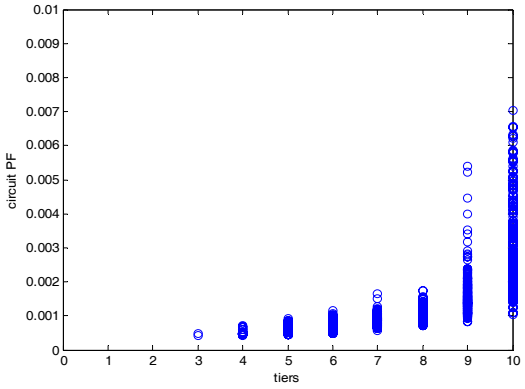

Fig. 3. Effect of tier count on circuit PF when device PF is 10^{-4}

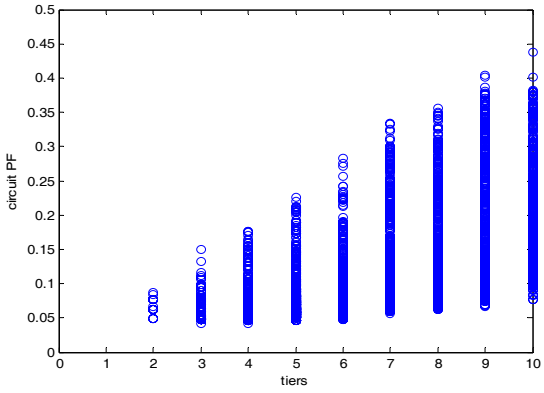

Fig. 4. Effect of tier count on circuit PF when device PF is 10^{-2}

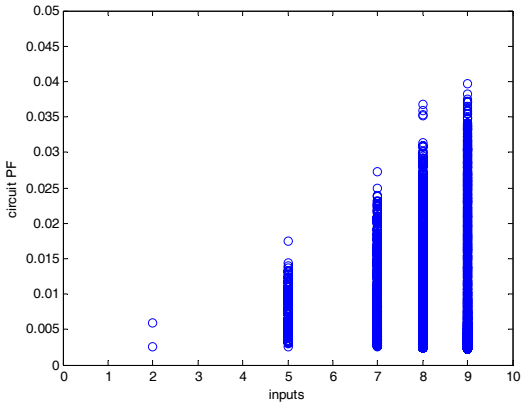

Fig. 5. Effect of input count on circuit PF when device PF is 10^{-4}

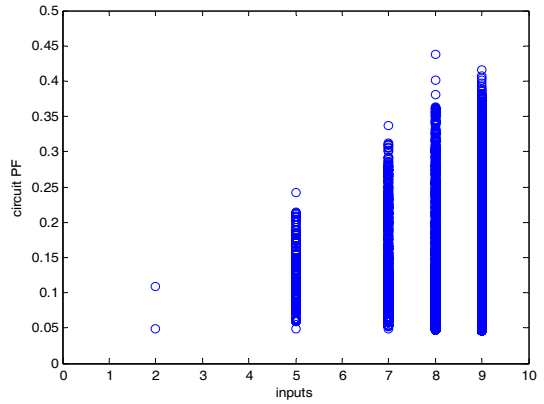

Fig. 6. Effect of input count on circuit PF when device PF is 10^{-2}

TABLE I
CORRELATIONS BETWEEN CIRCUIT CONFIGURATIONS AND THEIR PFS.

Correlation between	Device PF = 10^{-4}	Device PF = 10^{-2}
Gate count and circuit PF	0.9035	0.8930
Tier (level) count and circuit PF	0.8055	0.7010
Input (variable) and circuit PF	0.0752	0.0101

V. CONCLUSION

In this research, a Bayesian network based reliability-calculation tool was used to study the relationship of circuit topologies and the circuit reliability. Several thousand randomly generated combinational circuits (defined in Verilog) were created for this purpose. High degrees of positive correlations were found between gate counts and PFs, and between tier counts and PFs. Much lower correlation values were found between circuit variable counts and PFs. The authors are continuing their work of unraveling the non-linear and multi-variable relationship of circuit configuration to circuit reliability.

ACKNOWLEDGEMENT

This work was financially supported by the Research Affairs at the UAE University under a contract no. 02-02-9-11/08. Afzal Baig's contribution in data collection and processing is highly appreciated.

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